4. (Amended) Apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set.

5. (Amended) Apparatus as claimed in claim 1, wherein said instruction translator provides mapping states such that stack operands are added to or removed from said set of registers without moving stack operands between registers within said set of registers.

6. (Amended) Apparatus as claimed in claim 1, wherein said set of registers are operable to hold stack operands from a top portion of said stack including a top of stack operand from a top position within said stack.

7. (Amended) Apparatus as claimed in claim 1, wherein said stack further comprises a plurality of addressable memory locations holding stack operands.

9. (Amended) Apparatus as claimed in claim 7, wherein stack operands held within said plurality of addressable memory locations are loaded into said set of registers prior to use.

10. (Amended) Apparatus as claimed in claim 1, wherein said instruction translator uses a plurality of instruction templates for translating instructions from said second instruction set to instructions from said first instruction set.

12. (Amended) Apparatus as claimed in claim 1, wherein said instruction translator comprises one or more of:

(i) hardware translation logic;

(ii) instruction interpreting program code controlling a computer apparatus;

(iii) instruction compiling program code controlling a computer apparatus; and

(iv) hardware compiling logic.